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situ by heating a deposited titanium film 34 as a source material before further materials are deposited in the via hole 300. A titanium film 34 can be deposited by methods described earlier. After deposition of the titanium, the heating of the wafer can be conducted by transferring it in a vacuum to a heated pedestal where the titanium aluminide is formed, such as by using a CVD reactor-equipped cluster tool. Alternatively, the titanium film can be deposited in a single chamber using a heated pedestal to support the intermediate semiconductor workpiece such that titanium aluminide is formed rapidly as the elemental titanium is deposited on the exposed aluminum surface of aluminum conductor line 31. The dielectric layers 30 and 33 and the ARC layer 32 are of the same types as described in connection with FIG. 1.

In the Claims:

Please replace the respective original claims with the below amended claims.

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26. (Amended) A semiconductor device, comprising:
a metallic layer over a substrate;
an antireflective coating over said metallic layer;
a dielectric layer over said antireflective coating;
a via hole extending through the dielectric layer and said antireflective coating to a surface of the metallic layer;
a titanium aluminide layer lining at least a bottom of the via hole; and
a conductive material formed on the titanium aluminide layer.

27. (Amended) A semiconductor device, comprising:
an aluminum layer over a substrate;
a dielectric layer on the aluminum layer;
an antireflective coating over said dielectric layer;
a via hole extending through the dielectric layer and said antireflective coating to a surface of the aluminum layer;
a titanium aluminide layer lining at least a bottom of the via hole;

a titanium nitride layer substantially free of through cracks formed on the titanium aluminide layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the plug material.

28. (Amended) A semiconductor memory device, comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer on the first metallic layer;

an antireflective coating over said second dielectric layer;

a via hole extending through the second dielectric layer and the antireflective coating to a surface of the second metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer formed on the titanium aluminide layer;

a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material.

33. (Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a first metallic layer over a substrate;

a dielectric layer on the first metallic layer;

an antireflective coating over the dielectric layer;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the first metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer formed on the titanium aluminide layer;

a conductive plug material formed on the titanium compound layer; and

a second metallic layer on the dielectric layer and electrically connected to the plug material; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

34. (Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a metallic layer over a substrate;

a dielectric layer on the metallic layer;

an antireflective coating over said dielectric layer;

a via hole extending through the dielectric layer and said antireflective coating to a surface of the metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole; and

a conductive material formed on the titanium aluminide layer; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

35. (Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

an aluminum layer over a substrate;

a dielectric layer on the aluminum layer;

an antireflective coating over said dielectric layer;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the aluminum layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium nitride layer substantially free of through cracks formed on the titanium aluminide layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the plug material; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

36. (Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer on the first metallic layer;

an antireflective coating over the second dielectric layer;

a via hole extending through the second dielectric layer and the antireflective coating to a surface of the second metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer formed on the titanium aluminide layer;

a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

37. (Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a first metallic layer over a substrate;

a dielectric layer on the first metallic layer;

an antireflective coating over said dielectric layer;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the first metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer formed on the titanium aluminide layer;

a conductive plug material formed on the titanium compound layer; and

a second metallic layer on the dielectric layer and electrically connected to the plug material.

38. (Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a metallic layer over a substrate;

a dielectric layer on the metallic layer;

an antireflective coating over the dielectric layer;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the metallic layer;

a titanium aluminide liner at least a bottom of the via hole; and

a conductive material formed on the titanium aluminide liner.

39. (Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

an aluminum layer over a substrate;

a dielectric layer on the aluminum layer;

an antireflective coating over the dielectric layer;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the aluminum layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium nitride layer substantially free of through cracks formed on the titanium aluminide layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the plug material.

40. (Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer on the first metallic layer;

an antireflective coating over the second dielectric layer;

a via hole extending through the second dielectric layer and the antireflective coating to a surface of the second metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer formed on the titanium aluminide layer;

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a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material.